REMARKS

The Examiner rejected claims 1-20 under 35 U.S.C. 103(a) as being unpatentable over Yamagata (US 5,319,589) in view of Murakami (US 5,134,585).

The Examiner rejected claims 1-20 under 35 U.S.C. 103(a) as being unpatentable over Srinvasan (US 6,714,430) in view of Yamagata (US 5,319,589)

Applicants respectfully traverse the §103(a) rejections with the following arguments.

35 USC § 103 Rejections

First 35 USC Rejection

In Applicants response of July 5, 2005, Applicants supplied two sets of arguments for claim 17. Applicants believe that the Examiner has not addressed Applicants second argument concerning claim 17 which is repeated *infra*.

As to claims 1, 9, 17 the Examiner states that "Yamagata's "first bitline" and the replacement 'second bitline' (DTS) are non-adjacent, except in the case of one bitline (DT35)...Murakami discloses a memory array with bitline replacement using adjacent bitlines (Fig. 8), which is a well-known functional equivalent alternative to using a non-adjacent spare bitline for bitline replacement. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Yamagata's memory chip by replacing the non-adjacent bitline sparing with Murakami's adjacent bitline sparing. Such a substitution would have been obvious because Murakami's adjacent bitline sparing was already a well-known functional equivalent alternative."

First, Applicants contend the Examiner has not provided any evidence that adjacent bitline sparing is a well-known functional equivalent to non-adjacent bitline sparing and is an unsupported allegation. This is in violation of Smith v. Hayashi, 209 U.S.P.Q. 754, 759 ((Bd. Pat. App. & Int. 1980) which indicates the Examiner must provide evidence to support the prior art recognizes the equivalency. The Examiner has shown adjacent bitline sparing in the prior art, but not proof that it is recognized as an equivalent to non-adjacent bitline sparing.

Second, the Examiner further stated "Such a substitution is trivially simple to perform, and merely involves changing the connections to the switches SWO-SW35 such that the lower

position on each switch couples to the adjacent amplifier (901, in the case of SWO, etc.) instead of to the spare amplifier."

Applicants disagree with the Examiners assertion of triviality because changing the connections requires many logical and physical individual steps. (1) Each switch must be disconnected from a first common bus connecting to the amplifier driving spare bus DTS and from a second common bus connecting to the amplifier driving spare bus /DTS. (2) The first and second common buses must be removed as they are no longer needed. (3) Each amplifier must be connected to two switches instead of one. (4) Amplifier 900 must be connected to only the first switch.

Third, the switching network of Yamagata et al. is taught with each switch connected between a different data line and a different bitline context of a content addressable memory. The switching network of Murakami et al. is taught with each switch connected between the control signal and a pass gate in the context of a simple memory array. The adjacent-bitline sparing of the secondary reference Murakami et al. is not in taught in the same context as the primary reference Yamagata et al and therefore it is improper to combine the references.

Fourth, Applicants cannot find any teaching, suggestion or incentive for combining Yamagata and Murakami within Yamagata and Murakami. Absent such showing in the prior art, Applicants contend that the Examiner has impermissibly used the Applicants' teaching to hunt through the prior art for the claimed elements and combine them as claimed in violation of *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed Cir. 1991) which states "the suggestion and reasonable expectation of success must be founded in the prior art, not in the applicant's disclosure."

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 9 and 17 are not unpatentable over Yamagata et al. in view of Murakami et al and are in condition for allowance. Since claims 2-8 depend from claim 1, claims 10-16 depend from claim 9 and claims 18-20 depend from claim 17, Applicants respectfully maintain that claims 2-8, 10-16 and 18-20 are likewise in condition for allowance.

Applicants respectfully contend that claim 17, as amended, is not obvious in view of view of Yamagata et al. in view of Murakami et al. because view of Yamagata et al. in view of Murakami et al. does not teach or suggest every feature of claim 17. For example, Yamagata et al. in view of Murakami et al. does not teach or suggest "means for coupling each respective read line to a first respective read line or to a second respective read line based on said steering signal, said second respective read line being adjacent to said first respective read line." Applicants respectfully point out that Yamagata et al. is silent as to switching of read lines and Murakami et al. does not use read lines.

Based on the preceding arguments, Applicants respectfully maintain that claim 17 is not unpatentable over Yamagata et al. in view of Murakami et al and is in condition for allowance. Since claims 18-20 depend from claim 17, Applicants maintains claims 18-20 are likewise in condition for allowance.

Applicants respectfully contend that claim 18, as amended, is not obvious in view of view of Yamagata et al. in view of Murakami et al. because view of Yamagata et al. in view of Murakami et al. does not teach or suggest every feature of claim 18. In a first example, Yamagata et al. in view of Murakami et al. does not teach or suggest "means for directly

connecting each respective data line, after said respective data line has been connected to said second respective bitline, to a corresponding third respective bitline said third respective bitline immediately adjacent to said second respective bitline." Applicants point out that the switches of Yamagata et al. or Murakami et al. can only switch from a data line from a first bitline to a second bitline and cannot switch the data line from the second bitline to a third bitline. A second set of switches, coupled between the first set of switches and the bitlines, would be required and neither Yamagata et al. or Murakami et al. teach or suggest a second set of switches.

In a second example Yamagata et al. in view of Murakami et al. does not teach or suggest "means for directly connecting each respective read line, after said respective read line has been connected to said second respective read line, to a third respective read line, said third respective read line immediately adjacent to said second respective read line." Applicants point out that Yamagata et al. is silent as to switching of read lines and Murakami et al. does not use read lines.

Based on the preceding arguments, Applicants respectfully maintain that claim 18 is not unpatentable over Yamagata et al. in view of Murakami et al and is in condition for allowance.

Second 35 USC Rejection

As for claims 1-20 the Examiner states : "Srinivasan discloses a content-addressable memory (CAM) with one or more spare columns (i.e. spare "bitlines")...Yamagata discloses a CAM with a spare column. Yamagata teaches providing a circuit (500-535, 5S) that maintains a replaced bitline at a desired potential so that the replaced brine doesn't introduce noise in reading. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate Yamagata's replaced bitline potential-maintaining feature into Srinivasan's bitline replacement. Such incorporation would have been obvious because

Yamagata teaches that a replaced bitline potential-maintaining feature has an advantage of preventing the replaced bitline from introducing noise in reading.

As to claims 1-16, Applicants attach an Affidavit under 37 C.F.R. 1.131 stating conception and reduction to practice prior to the filing date of May 10, 2002 of United States Patent 6,714,430 to Srinivasan.

Applicants respectfully contend that claim 17, as amended, is not obvious in view of view of Srinivasan in view of Yamagata because Srinivasan in view of Yamagata does not teach or suggest every feature of claim 17. For example, Srinivasan in view of Yamagata does not teach or suggest "means for directing a first respective read line coupled to said first respective bitline to a second respective read line coupled to said second respective bitline in response to said steering signal." Applicants respectfully point out that Srinivasan and Yamagata are silent as to switching of read lines.

Based on the preceding arguments, Applicants respectfully maintain that claim 17 is not unpatentable over Srinivasan in view of Yamagata and is in condition for allowance. Since claims 18-20 depend from claim 17, Applicants maintains claims 18-20 are likewise in condition for allowance.

Applicants respectfully contend that claim 18, as amended, is not obvious in view Srinivasan in view of Yamagata because view of Srinivasan in view of Yamagata does not teach or suggest every feature of claim 18. In a first example, Yamagata et al. in view of Murakami et al. does not teach or suggest "means for directly connecting each respective data line, after said respective data line has been connected to said second respective bitline, to a corresponding third

respective bitline said third respective bitline immediately adjacent to said second respective bitline." Applicants point out that the switches of Srinivasan or Yamagata et al. can only switch from a data line from a first bitline to a second bitline and cannot switch not from the data line from the second bitline to a third bitline. A second set of switches, coupled between the first set of switches and the bitlines, would be required and neither Srinivasan or Yamagata et al teach or suggest a second set of switches.

In a second example Yamagata et al. in view of Murakami et al. does not teach or suggest "means for directly connecting each respective read line, after said respective read line has been connected to said second respective read line, to a third respective read line, said third respective read line immediately adjacent to said second respective read line." Applicants point out that both Srinivasan and Yamagata are silent as to switching read lines.

Based on the preceding arguments, Applicants respectfully maintain that claim 18 is not unpatentable over Srinivasan in view of Yamagata and is in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Batson et al.

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